REMARKS

Applicants appreciate the courtesy of the examiner in granting the interview which was conducted telephonically on July 17, 2008. During the interview, proposed amendments were discussed in relation to the art cited in the Office Action. The present amendment modifies the claims in the manner agreed by the parties during the interview as more clearly distinguishing the claimed invention from the art cited in the Office Action (over U.S. Patent No. 4,786,608 to Griffith ("*Griffith*"). During the interview, the examiner indicated that claim 1 as amended herein appears to be patentable over U.S. Patent No. 4,786,608 to Griffith ("*Griffith*") cited in the Office Action to reject the claims.

Claims 1, 2, 7, 8, and 27 through 32 are pending in the application with the present amendments. All of the pending claims continue to be readable on elected Species I (illustrated in FIG. 3). In the Office Action, all claims were rejected as being anticipated by U.S. Patent No. 4,786,608 to Griffith ("*Griffith*").

The objections to claims 7 and 29 are obviated by the present amendment of claim 1 which removes the clause "said second energy level having a value ranging from 10% less than said first energy level to said first energy level."

A few of the claims have been rejected under 35 U.S.C. §112 as allegedly failing to be supported by the original disclosure. The rejection of claim 1 is moot in view of the present amendment of claim 1, as discussed below. The rejection of claim 27 is also moot in view of the amendment to recite a BOX layer having a thickness of "at least 1350 angstroms and said BOX layer has *a first mini-breakdown* voltage greater than about 75 volts". These recitations are supported by FIG. 8.

Applicants traverse the other 35 U.S.C. §112 rejections on the following bases:

Regarding the language of claim 2 "said semiconductor layer of said substrate disposed above said BOX layer consists essentially of single crystal silicon", support for this recitation is found in paragraphs [0004] and [0021]. Paragraph [0004] simply states what is common knowledge: "SOI substrates have a structure in which an active device layer of single crystal silicon is formed over an insulating layer of the substrate." Paragraph [0021], in referring to FIG. 2, indicates that "the SIMOX process is optimized for a nominal silicon-on-insulator layer 230" of the SOI wafer. Paragraph [0022] references the BOX layer 220 which immediately underlies the silicon-on-insulator layer 230 in FIG. 2. Thus, it is clear that the "silicon-on-insulator layer" is given its ordinary meaning consistent with paragraph [0004], this layer being the "active device layer of *single crystal silicon* . . . formed over an insulating layer of the substrate. "

Regarding the language of claim 8 "said first dose is less than or equal to $4 \times 10^{17} cm^{-2}$" is supported by the specification at paragraph [0021] which states "The implant does is preferably in the range of $1x10^{16}$ *to* $4x10^{17}$ *ions/cm*^{2}.

Regarding the language of claim 28, "up to a nominal thickness of 700 angstroms" is supported by the original specification at paragraph [0021] which states a "nominal silicon-on-insulator layer 230 thickness of between 550 angstroms *and 700 angstroms. . . .*"

In the Office Action, claims 1-2, 7-8 and 22 were rejected under 35 U.S.C. 102(b) as allegedly anticipated by *Griffith* or under 35 U.S.C. §103(a) as being obvious

over *Griffith*. For the reasons set forth below, applicants respectfully submit that the presently pending claims overcome the rejections over *Griffith*.

Claim 1 now recites annealing to form a BOX layer having an upper major surface adjoining a single crystal semiconductor layer of the substrate disposed above the BOX layer and the BOX layer having a lower major surface adjoining a single-crystal semiconductor region of the substrate disposed below the BOX layer. Claim 1 now also recites that the BOX has a greater first mini-breakdown voltage for thicknesses of the BOX layer of between at least about 500 angstroms and about 1400 angstroms. The present amendments to claim 1 are supported by FIG. 2 and the accompanying description of the wafer structure in paragraphs [0021] and [0022] which show a BOX layer 220 having a lower major surface adjoining the single crystal silicon substrate 200, and having an upper major surface adjoining a semiconductor layer 230 disposed above the BOX layer. In addition, as referred to in paragraph [0032], FIG. 8 teaches that the improved SIMOX BOX has a greater first mini-breakdown voltage between at least the BOX layer thicknesses of 500 angstroms and 1400 angstroms for which data points are shown in FIG. 8. Applicants also note that, given the great gap between the first mini-breakdown voltage shown for the improved SIMOX BOX versus the old SIMOX BOX in FIG. 8 at a thickness of 1400 angstroms and the fact that the slopes of the two curves are roughly the same, one can expect the claimed process to yield a BOX layer with a greater first mini-breakdown for thicknesses even greater than 1400 angstroms. Moreover, the recitation that the BOX layer has "a greater first mini-breakdown voltage" is supported directly by FIG. 8. or example, for every thickness between at least about 500 angstroms and about 1400 angstroms.

The invention recited in claim 1 is not disclosed by *Griffith*. *Griffith* merely describes an unusual approach to making wafers which have a polysilicon "electric field shielding layer (EFS) 32" (col.4 ll.61-64) sandwiched between two oxide layers 13, 33, (FIG. 4) In *Griffith*, an upper major surface of the BOX layer 13 does not adjoin a single-crystal semiconductor layer (claim 1) (or as in claim 2, single-crystal silicon-on-insulator layer of a substrate). Instead, in *Griffith*, the upper major surface of the BOX layer adjoins the polysilicon EFS layer 32. (col.4 ll.61-68, col.5 ll.13-20). Another SiO_2 layer is disposed between the EFS layer and the "annealed top surface crystalline silicon layer 14." (*Id.*). Also, *Griffith* does not teach that a BOX layer is formed which has a first mini-breakdown voltage that is greater for thicknesses of the BOX layer of between at least about 500 angstroms and about 1400 angstroms.

Applicants point out the particular recitations in each of claims 8, 27, 28, 29 and 30, each of which independently distinguishes such claims from *Griffith*.

With respect to claim 31, *Griffith* fails to teach the use of internal thermal oxidation (ITOX) (see paragraphs [0022] and [0025] of applicants' specification) to form the BOX layer. There is no reference to ITOX in *Griffith*.

With respect to claim 32, *Griffith* fails to teach performing the annealing at a temperature of about 1320 °C. At most, *Griffith* teaches annealing at a temperature between about 1150 and 1250 °C. Support for claim 32 is provided in paragraph [0032] of applicants' specification.

In view of the amendments and remarks herein, it is believed that all claims of the application are now in condition for allowance. However, if for any reason the Examiner does not believe that such action can be taken at this time, the Examiner is

requested to telephone the applicants' attorney at the number indicated below to discuss any issues that may remain.

It is believed that no fees are required in connection with the filing of the present amendment. However, if any fee is due in connection with this amendment, authorization is granted to debit the Deposit Account No. 09-0458 of the Assignee. If there is an overpayment, please credit the same account.

Respectfully submitted,
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